

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 250386US2		SERIAL NO. <u>10/799,780</u> New Application	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Satoshi INABA, et al.			
				FILING DATE Herewith		GROUP <u>2818</u>	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
TH	AA	6,525,403	02/25/03	Satoshi INABA, et al.			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
TH	AO	7-202146	08/04/95	Japan (with English Abstract)		x	
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
TH	AW	Yang-Kyu CHOI, et al., "Sub-20nm CMOS FinFET Technologies", INTERNATIONAL ELECTRON DEVICES MEETING (IEDM) TECH. DIG., December 2001, pgs. 421-424					
	AX	Bin YU, et al., "FinFET Scaling to 10nm Gate Length", INTERNATIONAL ELECTRON DEVICES MEETING (IEDM) TECH. DIG., December 2002, pgs. 251-254					
	AY						
	AZ					<input type="checkbox"/> Additional References sheet(s) attached	
Examiner <u>TH-TH-HO</u>					Date Considered <u>NOV 2005</u>		
<small>*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>							